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Design of CMOS Programmable Switched Capacitor Equalizer Using 0.18µm Technology

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1. Abstract

In this paper describes design of three operational amplifier, transmission gate and capacitor banks to independently control , bandwidth, and the peak voltage gain steps for the dip frequency response. The equalizer located at the receiver removes the effects of ISI, CCI, burst noise interference and attempts to recover the transmitted symbols. It has been seen that linear equalizers show poor performance, where as nonlinear equalizer provide superior performance. Since a considerable part of the power consumption is due to the analog baseband filters, improved and novel analog filter design approaches have to be developed. We design of versatile and economical switched capacitor equalizing structure to compensate attenuation characteristics is presented. To demonstrate the proposed techniques, a ±1.8V, fabricated in a conventional 0.18µm CMOS process is presented. The op-amp achieves unity GAIN bandwidth of 80.76dB which is used to implement analog filters, mainly in the audio frequency range, is by means of switched capacitor circuit. The measured power consumption for the filter alone consumes about 0.74mW for a supply voltage of ± 1.8V. Design, simulation and layout of the circuit is done in Cadence spectre environment with UMC 0.18µm CMOS process.

Keywords

Analog IC design, op-amp, transmission gate, channel equalization, programmable switched capacitor equalizer

2. Introduction

A programmable switched capacitor as transmitter pulse-shaping filters, receiver equalizers, echo cancellers, anti-aliasing filters, modulators, decimation filters, and others. The preferred technology for implementation is typically digital due to the high accuracy attainable. However, filters implemented in this technology tend to consume significant
power and achieve processing speeds below those attainable using analog implementations. Thus, for low-cost, high-speed applications designers tend to favor analog filters. However, these filters suffer from process variations, operating temperature, and parasitic effects; hence, tuning is essential.

The proposed switched capacitor variable attenuation equalizer architecture is not directly based on the bode-type realizations. It is based on the implementation of the transfer function, in the z domain, of the attenuation equalizer. A CMOS test structure using 0.18µm technology. The resulting implementation must have a minimum number of active components. The equalizer architecture is based on the following observation:-

- The canter frequency is determined by double integration loop;
- The bandwidth BW and gain coefficient A_1 are given by a single integration loop; and
- The equalizer architecture can be visualized as composed of a low-pass and high-pass filter with unity gain, and band-pass filter with a peak voltage gain T_0.

3. Circuit Implementation

3.1 OP AMP Design:

The circuit provides good voltage gain, a good common-mode range and good output swing. Before the analysis of the op-amp is done, some of the basic principles behind the working of MOS transistors are reviewed. The first stage in Fig.3.1 consists of a p-channel differential pair M_1-M_2 with an n-channel current mirror load M_3-M_4 and a p-channel tail current source M_5. The

second stage consists of an n-channel common-source amplifier M_{10} with a p-channel current-source load M_6. The sizes of the transistors were designed for a bias current of 413.2µA to provide for sufficient output voltage swing, output-offset voltage, slew rate, and gain-bandwidth product.

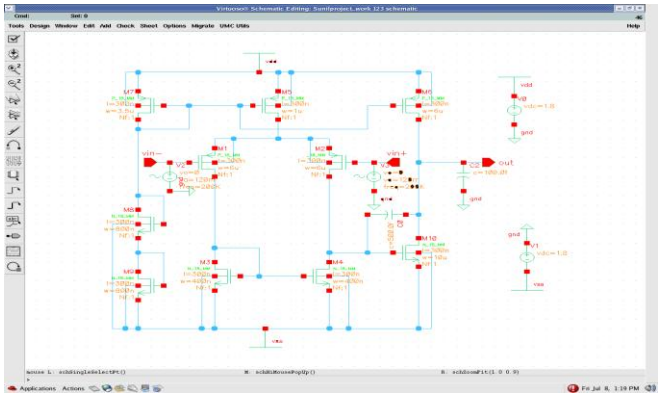


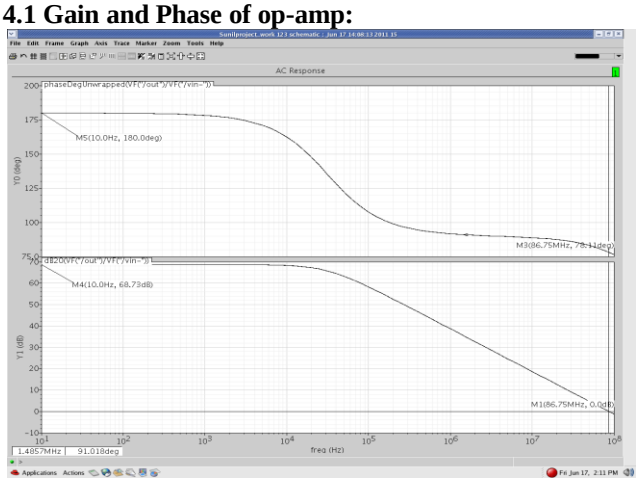
Figure 3.1 Schematic of CMOS Op-Amp

S. NO.	DEVICE	W/L( )
1	M1, M2 ,M6	06/0.3
2	M3, M4	0.4/0.3
3	M5	01/0.3
4	M7	3.5/0.3
5	M8, M9	0.8/0.3
6	M10	10/0.3

Table3.1 Transistor sizing for CMOS Op-amp Design

4. Result of op-amp

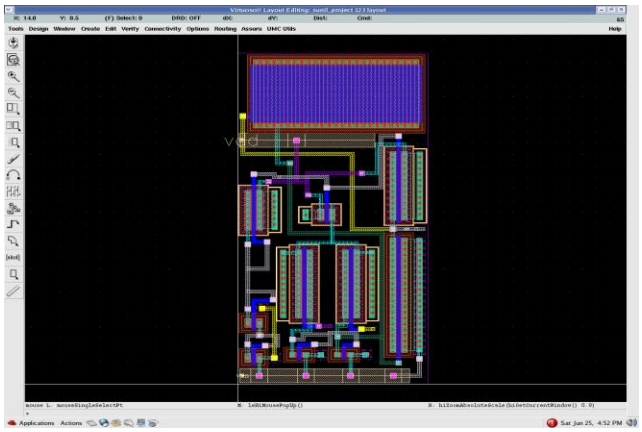
4.1 Gain and Phase of op-amp:



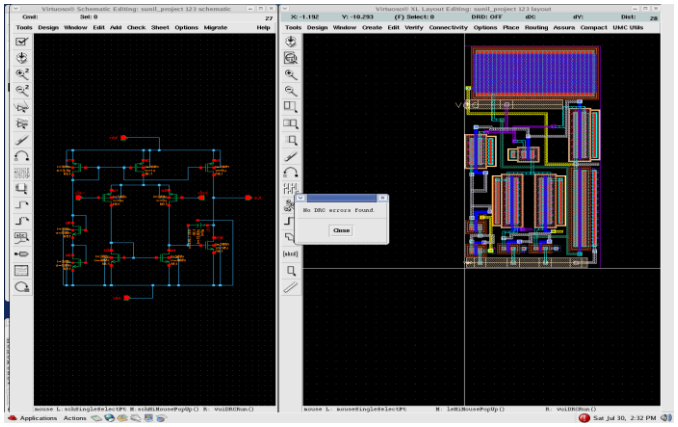
S.NO.	Experimental	Results Value
1	Open Loop Gain	68.76dB
2	3dB Frequency	31.41kHz
3	Unity Gain Frequency	86.76MHz
4	Slew Rate	2.344V/
5	Power Dissipation	0.74mW
6	Load Capacitance	0.1pF
7	C_c	500.0fF
8	PSRR	80dB
9	CMRR	91dB

Tab.4.1 SUMMARY OF EXPERIMENTAL RESULTS

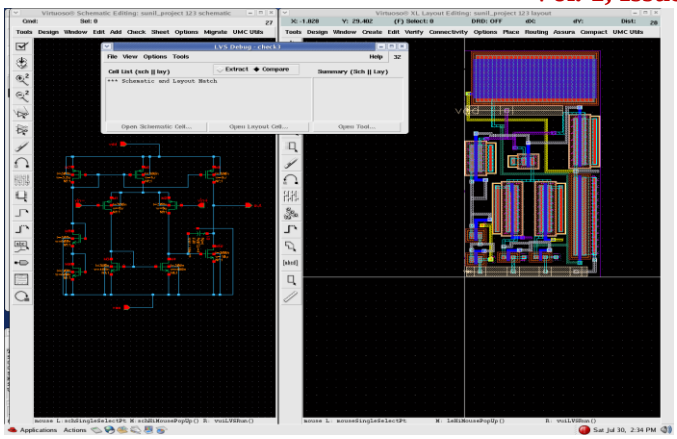
4.2 Layout of op-amp:



4.3 DRC (Design Rule Check) of op-amp:



4.4 LVS Report of op-amp



5. Transmission gate

The operating and control switches were implemented by CMOS transmission gates. The dimensions of the switches, the *W/L's,* of PMOS and NMOS transistors are 0.24 m/0.18 m. The clock generator is a non overlapping clock. Both complementary clock phases for the p-channel and n-channel switches are obtained when the clock generator circuit is triggered by a single clock.

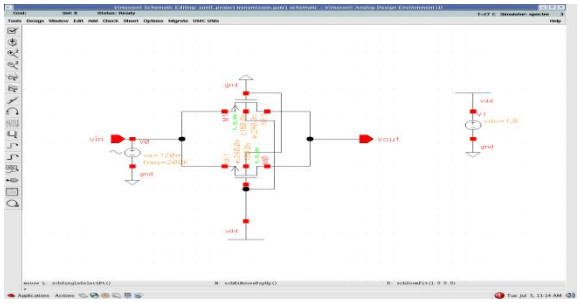


Figure 5.1 Transmission gate

6. Architecture of programmable switched capacitor equalizer

The three amplifiers used for the bump equalizer plus an additional test amplifier for measurement purposes. A unity-gain output buffer and unity-gain test-buffer amplifiers, contains in a clockwise direction, the control switches for f_o, k, and Q, respectively. Each variable (f_0, k, Q) is programmed by four external control bits. Capacitor banks and their operating switches are illustrated. Finally, the non-overlapping clock generator is shown. The op-amp structure used is a trans-conductance amplifier similar to the one reported in the structure includes transistors to improve the dc gain and PSRR. The basic characteristics of the designed amplifier obtained from SPICE simulations and measurements. . The central frequency f_0 can change from 0 to 7.7 MHz when the clock frequency is 75 kHz.

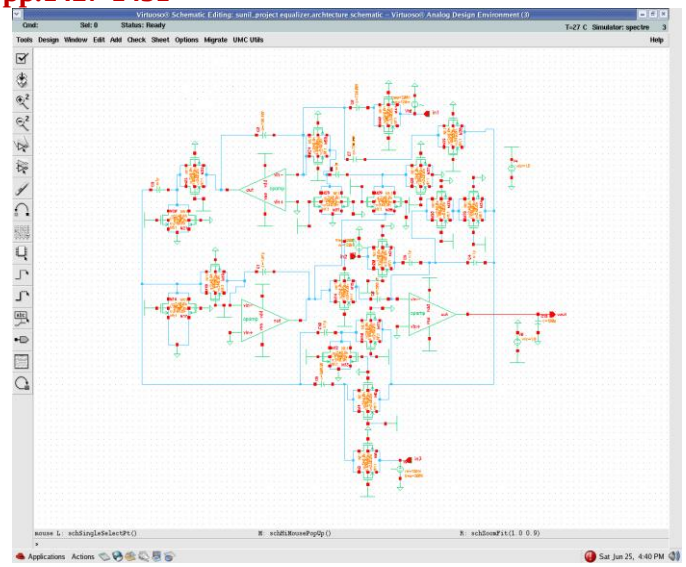


Figure 6.1 programmable switched capacitor equalizer

Other capacitor bank architectures can be considered to generate frequency responses with a constant step distribution of f_0 over the entire programming range. However, and as a consequence of the nonlinear capacitance step required, two disadvantages of the last array architecture are that the number of bits must be equal to the number of steps and that there is an increased capacitor spread. For that reason, a different implementation was made for the bank k_{C1}. This structure is sensitive to bottom-plate capacitance and bump amplitudes are not equidistant. An advantage of this implementation is moderated "reduced" values of the capacitor C_1 and, of course, the bank C_l/ .

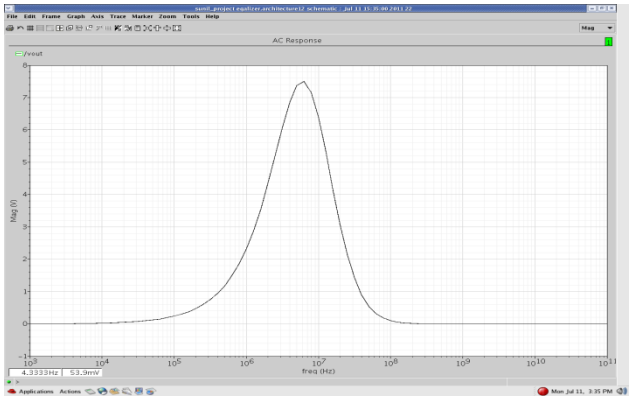


Figure 6.2 centre frequency SC equalizer

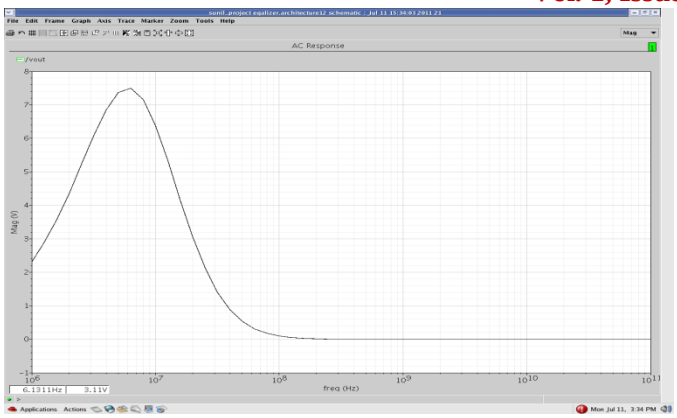


Figure 6.3 Bandwidth Programmability of the SC Equa.

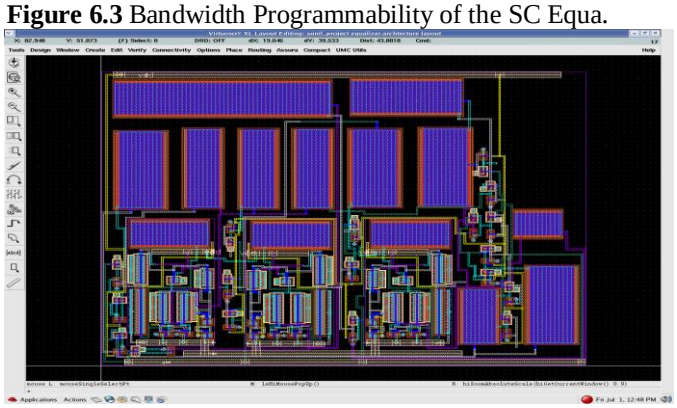


Figure 6.4 layout of programmable SC equalizer

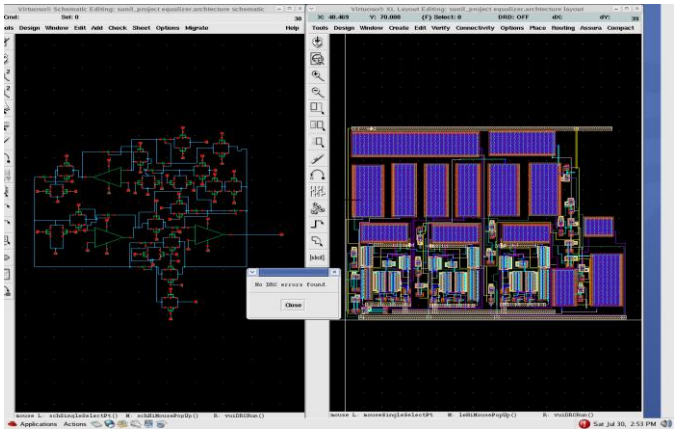


Figure 6.5 DRC (Design Rule Check) of programmable SC equalizer

7. Conclusion

It is the schematic of CMOS op-amp using SC Equalizer. It has Open Loop Gain 68.76dB.A unity gain bandwidth is obtained 80.76MHz. Phase margin is the phase difference between phases of Av (W 0dB) and -180˚ where W 0dB is the frequency at which | Av| is unity, called unity gain frequency. The phase margin is obtained 78.11 degree. The sizes of the transistors were designed for a bias current of 413.2µA to provide for sufficient output voltage swing, output-offset voltage, slew rate, and gain-bandwidth product. There is the plot of power supply rejection ratio. It recognized that the change in output with power supply is 80dB.The common mode rejection ratio was found to be 91dB. The measured value of slew rate is 2.344 V/µs. Power Dissipation is .74mW. The central frequency f_0 can change from 0 to 7.7 MHz when the clock frequency is 75 kHz. Then finally Layout of CMOS Programmable-SC Equalizer.

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